ABSTRACT OF THE DISCLOSURE

A buffer (40) includes a capacitor (42) having a first terminal for receiving an input signal, and a second terminal; a first transistor (44) having a first current electrode for receiving a first power supply voltage, a control electrode coupled to the second terminal of the capacitor (42), and a second current electrode for providing an output signal of the buffer (40); and a second transistor (45) having a first current electrode coupled to the second current electrode of the first transistor (44), a control electrode coupled to the second terminal of the capacitor (42), and a second current electrode for receiving a second power supply voltage. A capacitance of the capacitor (42) is chosen to reduce a peak-to-peak voltage swing of the input signal such that a peak-to-peak voltage swing at the control electrodes of the first (44) and second (45) transistors is less than or equal to a difference between the first and second power supply voltages.